CLAIMS

What is claimed is:

1.A method for forming a self-aligned trench, said method comprising:

providing a semiconductor substrate having a first hard mask layer thereon and openings therein, wherein a capacitor is formed in the interior of said opening of said semiconductor substrate;

conformally forming a second hard mask layer on said first hard mask layer and said capacitor;

forming an insulator layer on said second hard mask layer;

forming a pattern photoresist layer on said insulator layer; and

removing parts of said insulator layer, said second hard mask layer, said first hard mask layer and said semiconductor substrate, with a part of said insulator layer as a mask, to form a trench in the middle between partial said two capacitors, wherein a different removing rate exists between said insulator layer and said second hard mask layer.

2.The method of claim 1; further comprising:

forming an isolation into said trench.

3.The method of claim 2, wherein said isolation comprises an oxide.

4.The method of claim 2, wherein the depth of said trench is about 3000-4000 angstroms.

5.The method of claim 1, wherein steps of providing said semiconductor substrate comprise:

doping a buried layer into said semiconductor substrate, wherein a doping type of said buried layer is different from the doping type of said semiconductor substrate;

forming a buffer layer and said first hard mask layer sequentially on a surface of said semiconductor substrate;

forming a photoresist which has holes on a surface of said first hard mask layer to expose said first hard mask layer; and

removing parts of said first hard mask layer, said buffer layer and said semiconductor substrate to form said openings.

6.The method of claim 5, wherein said buffer layer comprises an oxide layer.

7.The method of claim 1, wherein steps of forming said capacitor comprise:

forming a lower electrode diffused into a lower portion of said opening of said semiconductor substrate;

forming a first dielectric layer and an upper electrode filled into said lower portion of said opening of said semiconductor substrate;

forming a dielectric collar layer on a side-wall of said opening above said upper electrode, wherein said dielectric collar layer covers an exposed surface of said first dielectric layer within said opening but not fully covers said exposed surface of said upper electrode; and

forming an internal electrode on both said dielectric collar layer and said

upper electrode.

8.The method of claim 1,wherein the depth of said opening is about 7-8μm.

9.The method of claim 1, wherein buried straps exist in the joins of a side-wall of said opening and a surface of said semiconductor substrate.

10.The method of claim 9, wherein said capacitor is conducted with a CMOS transistor via said buried straps and said internal electrode.

11.The method of claim 1, wherein the thickness of said second hard mask layer is about one third to one sixth width of said opening.

12.The method of claim 1, wherein said pattern photoresist layer defines an active area (AA) and a device area via mask alignment process.

13.The method of claim 12, wherein a CMOS transistor is further fabricated in said device area.

14.The method of claim 1, wherein said first hard mask layer comprises a nitride layer.

15.The method of claim 1, wherein said second hard mask layer comprises a bottom anti-reflective coating (BARC).

16.The method of claim 1, wherein said insulator layer comprises a dielectric layer.

17.The method of claim 1, wherein said different removing rate is a selectivity of etching away said insulator layer with respect to said second hard mask layer of more than 8 to 1.

18.A method for forming a self-aligned trench isolation, said method comprising:

providing a semiconductor substrate having a pad nitride layer thereon and openings therein, wherein a capacitor is formed in the interior of said opening of said semiconductor substrate;

conformally forming a hard mask layer on said pad nitride layer and said capacitor;

forming a dielectric layer on said hard mask layer;

forming a pattern photoresist layer on said dielectric layer;

removing parts of said dielectric layer, said hard mask layer, said pad nitride layer and said semiconductor substrate, with a part of said dielectric layer as a mask, to form a trench in the middle between partial said two capacitors, wherein a removing rate between said dielectric layer and said hard mask layer is different; and

filling an insulator into said trench to form a trench isolation.

19.The method of claim 18, wherein steps of providing said semiconductor substrate comprise:

doping a buried layer into said semiconductor substrate, wherein a

doping type of said buried layer is different from the doping type of said semiconductor substrate;

forming a pad oxide layer and said pad nitride layer sequentially on a surface of said semiconductor substrate;

forming a photoresist which has holes on a surface of said pad nitride layer to expose said pad nitride layer; and

removing parts of said pad nitride layer, said pad oxide layer and said semiconductor substrate to form said openings.

20.The method of claim 18, wherein steps of forming said capacitor comprise:

forming a lower electrode diffused into a lower portion of said opening of said semiconductor substrate;

forming a first dielectric layer and an upper electrode filled into said lower portion of said opening of said semiconductor substrate;

forming a dielectric collar layer on a side-wall of said opening above said upper electrode, wherein said dielectric collar layer covers an exposed surface of said first dielectric layer within said opening but not fully covers said exposed surface of said upper electrode; and

forming an internal electrode on both said dielectric collar layer and said upper electrode.

21.The method of claim 18, wherein the depth of said opening is about 7-8μm.

22.The method of claim 18, wherein buried straps exist in the joins of a

side-wall of said opening and a surface of said semiconductor substrate.

23.The method of claim 22, wherein said capacitor is conducted with a CMOS transistor via said buried strap and said internal electrode.

24.The method of claim 18, wherein the thickness of said hard mask layer is about one third to one sixth width of said opening.

25.The method of claim 18, wherein said pattern photoresist layer defines an active area (AA) and a device area via mask alignment process.

26.The method of claim 25, wherein a CMOS transistor is further fabricated in said device area.

27.The method of claim 18, wherein said hard mask layer comprises a bottom anti-reflective coating (BARC).

28.The method of claim 18, wherein said removing rate between said dielectric layer and said hard mask layer is a selectivity of etching away said dielectric layer with respect to said hard mask layer of more than 8 to 1.

29.The method of claim 18, wherein said insulator comprises an oxide.

30.The method of claim 18, wherein the depth of said trench is about 3000-4000 angstroms.